WHAT IS CLAIMED IS:

1. A programmable logic device comprising:

a plurality of logic array blocks;

a programmable interconnect bus, programmably coupled to the plurality of logic array blocks;

a tristate bus; and

a plurality of tristate devices, coupled between the plurality of logic array blocks and the tristate bus, wherein the plurality of tristate devices couple and decouple the logic array blocks to the tristate bus.

2. The programmable logic device of claim 1 further comprising:

a plurality of OE generation circuits, coupled to the plurality of tristate devices, the plurality of OE generation circuits controlling the plurality of tristate devices.

3. The programmable logic device of claim 2 wherein a logic array block programmably couples to drive the plurality of OE generation circuits.

4. The programmable logic device of claim 1 further comprising:

a tristate bus driver, coupled between the tristate bus and the programmable interconnect bus, for driving signals between the tristate bus and programmable interconnect bus.

5. A programmable logic device comprising:

a programmable interconnect bus; and

a logic array block, comprising:

a plurality of logic elements configurable to perform logical functions;

a plurality of tristate drivers, coupled between the plurality of logic elements and the programmable interconnect bus; and

tristate control logic controlling states of the plurality of tristate drivers.

6. The programmable logic device of claim 5 wherein the plurality of tristate drivers are programmably enabled to couple the plurality of logic elements to the programmable interconnect bus.

7. The programmable logic device of claim 5 wherein the tristate control logic is programmably coupled to signals on the programmable interconnect bus for controlling the states of the plurality of tristate drivers.

8. The programmable logic device of claim 5 wherein one of the plurality of logic elements is coupled through one of the plurality of tristate drivers through the programmable interconnect bus to another one of the plurality of logic elements.

9. A tristate driver for an integrated circuit comprising:

a data input;

an enable control node;

a first driver transistor, coupled between a first potential source and an output node;

a second driver transistor, coupled between the output node and a second potential source;

a first predriver comprising:

a first transistor, coupled between the first potential source and a control electrode of the first driver transistor, having a control electrode coupled to an inversion of the enable input;

a second transistor, coupled between the control electrode of the first electrode driver transistor and control of the second driver transistor, having a control electrode coupled to the inversion of the enable input; and

a third transistor, coupled between the control electrode of the second driver transistor and the second potential source, having a control electrode coupled to the enable input; and

a second predriver comprising:

a first transistor, coupled between the first potential source and the control electrode of the first driver transistor, having a control electrode coupled to the data input;

a second transistor, coupled between the control electrode of the first driver transistor and the control electrode of the second driver transistor, having a control electrode coupled to the enable input; and

a third transistor, coupled between the control electrode of the second driver transistor and the second potential source, having a control electrode coupled to the data input.

10. The tristate driver of claim 9 further comprising:

an enable control, generating an output signal at the enable control node for programmably enabling and programmably disabling the tristate driver.